CDA 4203L Sec 001

Computer System Design Lab

Lab 2 Report

Verilog Based ALU Design

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| --- | --- |
| Today’s Date: | 2/9/18 |
| Your Name: | Boyang Wu |
| Your U Number: | U95035892 |
| No. of Hours Spent: | 12 |
| Exercise Difficulty:  (Easy, Average, Hard) | Average |
| Any Other Feedback: | A bit trickier in the structural part |

Problem 1: ALU Behavioral Verilog

Problem 1: Verilog Test Bench

Problem 1: Simulation Waveforms (add as many pages as you need).

Include *atleast* two test vectors per function. For example, demonstrate through the waveforms, that the ALU performs inversion correctly on two inputs, say, 0010 and 1111.

Problem 2: Behavioral Components (insert 1 page per component)Problem 2: ALU Structural Verilog (Use as many pages as needed.)

Problem 2: Verilog Test Bench

Problem 2: Simulation Results

Include *atleast* two test vectors per function. For example, demonstrate through the waveforms, that the ALU performs inversion correctly on two inputs, say, 0010 and 1111.